Notice of Allowability	Application No.	Applicant(s)	
	10/028,319	ITO ET AL.	
	Examiner	Art Unit	
	Kibrom K. Gebresilassie	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *05/30/2006*.

2. ☒ The allowed claim(s) is/are *1,3-5,7-9,11-13 and 15-17*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☒ Certified copies of the priority documents have been received in Application No. *10/028,319* .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 12/28/01
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *09/29/2006* .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

KAMINI SHAH
SUPERVISORY PATENT EXAMINER

DETAILED ACTION

1. This Office Action responsive to amended application filed on May 30, 2006.

2. Claims 2, 6, 10, and 14 are cancelled.

3. Claims 1, 3-5, 7-9, 11-13, and 15-17 are examined.

Continued Examination Under 37 CFR 1.114

4. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on May 30, 2006 has been entered.

EXAMINER'S AMENDMENT

5. Authorization for this examiner's amendment was given in a telephone interview with attorney Joseph Wrkich on September 09/29/2006.

a. Claims 1, 4, 8, 9, 12, 16, and 17 have been amended as follows:

Claim 1 (Currently Amended):

A method of simulation for designing a semiconductor device with simulation data of the semiconductor device, comprising:

determining whether or not the simulation data includes boundary conditions set for a boundary of a calculation area set for the simulation;

computing ~~the~~ an influence of the boundary conditions on ~~the~~ an inside of the calculation area if the simulation data include the boundary conditions;

displaying the influence of the boundary conditions on the inside of the calculation area, said displaying operation comprising:

if the simulation data includes the boundary conditions, generating mirror images outside the calculation area according to the boundary conditions; and

displaying the mirror images, as well as real images included in the calculation area;

prompting to enter an instruction whether or not the boundary conditions are changed; and

if an instruction to make no change in the boundary conditions is entered, carrying out the simulation with the simulation data.

Claim 4 (Original):

The method as claimed in claim 3, further including:

computing and displaying ~~the~~ an influence of other boundary conditions on the calculation area.

Claim 8 (Original):

The method as claimed in claim 1, wherein computing and displaying the influence of the boundary conditions includes:

computing and displaying information about ~~the~~ accuracy and speed of the simulation to be carried out with the simulation data including the boundary conditions.

Claim 9 (Currently Amended):

A computer program product for simulation for designing a semiconductor device with simulation data of the semiconductor device, comprising:

a determining module configured to determine whether or not the simulation data includes boundary conditions set for a boundary of a calculation area set for the simulation if the simulation data includes the boundary conditions;

a computing module configured to compute ~~the~~ an influence of the boundary conditions on ~~the~~ an inside of the calculation area if the simulation data include the boundary conditions;

a displaying module configured to display the influence of the boundary conditions on the inside of the calculation area, said displaying module comprising:

a generating module configured to generate images outside the calculation area according to the boundary conditions if the simulation data includes the boundary conditions; and

an image displaying module configured to display the mirror images, as well as real images included in the calculation area;

a prompting module configured to prompt to enter an instruction whether or not the boundary conditions are changed; and

a simulation module configured to carry out the simulation with the simulation data if an instruction to make no change in the boundary conditions is entered.

Claim 12 (Original):

The program product as claimed in claim 11, further comprising:

a computing and displaying module configured to compute and display ~~the~~ an influence of other boundary conditions on the calculation area.

Claim 16 (Previously Presented):

The program product as claimed in claim 9, wherein displaying module includes:

displaying information about ~~the~~ accuracy and speed of the simulation to be carried out with the simulation data including the boundary conditions.

Claim 17 (Currently Amended):

A semiconductor device manufacturing method, comprising:

designing a semiconductor device;

outputting design data of the semiconductor device;

simulating the design data of the semiconductor device employing a simulation data in connection with the semiconductor device, the simulating comprising:

determining whether or not the simulation data includes boundary conditions set for a boundary of a calculation area set for the simulation;

computing ~~the~~ an influence of the boundary conditions on ~~the~~ an inside of the calculation area if the simulation data includes the boundary conditions;

displaying the influence of the boundary conditions on the inside of the calculation area, said displaying operation comprising:

if the simulation data includes the boundary conditions, generating mirror images outside the calculation area according to the boundary conditions; and

displaying the mirror images, as well as real images included in the calculation area;

prompting to enter an instruction whether or not the boundary conditions are changed; and

if an instruction to make no change in the boundary conditions is entered, carrying out the simulation with the simulation data; and

fabricating the semiconductor device according to the design data.

Allowable Subject Matter

1. Claims 1, 3-5, 7-9, 11-13, and 15-17 are allowed.

2. The following is an examiner's statement of reasons for allowance:

a. Regarding claims 1, 9, and 17, the prior art of record fail to teach singly or in combination with another prior art the limitation of "if the simulation data includes the boundary conditions, generating mirror images outside the calculation area according to the boundary conditions; and displaying the mirror images, as well as real images included in the calculation area."

Conclusion

3. Any inquiring concerning this communication or earlier communication from the examiner should be directed to Kibrom K. Gebresilassie whose telephone number is (571) 272-8571. The examiner can normally be reached on Monday-Friday, 8:30 am to 4:30 pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner supervisor, Kamini shah can be reached at (571) 272-2279. The official fax number is (571) 273-8300. Any inquiring of a general nature relating to the status of this application should be directed to the group receptionist whose telephone number is (571) 272-3700.

KAMINI SHAH
SUPERVISORY PATENT EXAMINER